WHAT IS CLAIMED IS:

1. A method of manufacturing an inter-level dielectric (ILD) layer of a semiconductor device, the method comprising:

forming a first low-dielectric constant material sub-layer over the substrate, the first low-dielectric constant material having at least one first material property;

forming a second low-dielectric constant material sub-layer over the first low-dielectric constant material sub-layer, the second low-dielectric constant material sub-layer having at least one second material property, wherein the at least one second material property is different from the at least one first material property; and

forming a third low-dielectric constant material sub-layer over the second low-dielectric constant material sub-layer, the third low-dielectric constant material sub-layer having at least one third material property, the at least one third material property being different from the at least one second material property.

2. The method according to Claim 1, wherein forming the ILD layer comprises forming the first low-dielectric constant material sub-layer, second low-dielectric constant material sub-layer, and third low-dielectric constant material sub-layer from methylsilsesquioxane (MSQ), a MSQ derivative, hydridosilsesquioxane (HSQ), a HSQ derivative, an oxide and MSQ hybrid, a porogen/MSQ hybrid, an oxide and HSQ hybrid, a porogen/HSQ hybrid, or combinations thereof.

3. The method according to Claim 1, wherein forming the ILD layer comprises forming the first low-dielectric constant material sub-layer, second low-dielectric constant material sub-layer, and third low-dielectric constant material sub-layer continuously from the same material in one or more deposition chambers.

4. The method according to Claim 1, wherein forming the ILD layer comprises forming the first low-dielectric constant material sub-layer, second low-dielectric constant material sub-layer, and third low-dielectric constant material sub-layer while adjusting the deposition conditions.

5. The method according to Claim 4, wherein adjusting the deposition conditions comprises adjusting the gas flow rate, power, or gas species.

6. The method according to Claim 1, wherein the first material property, second material property, and third material property comprise density, dielectric constant, adhesion, or Young's modulus.

7. The method according to Claim 1, further comprising forming at least one fourth low-dielectric constant material sub-layer over the third low-dielectric constant material sub-layer, the fourth low-dielectric constant material sub-layer having at least one fourth material property, wherein the at least one fourth material property is different from the at least one third material property.

8. A method of manufacturing a semiconductor device, the method comprising:

providing a substrate, the substrate having component regions formed thereon;

forming a first etch stop layer over the substrate;

forming a first ILD layer over the first etch stop layer; and

forming at least one first conductive region in the first ILD layer and first etch stop layer, wherein at least one first conductive region makes electrical contact with at least one component region of the substrate, and wherein forming the first ILD layer comprises:

forming a first low-dielectric constant material sub-layer over the first etch stop layer;

forming a second low-dielectric constant material sub-layer over the first low-dielectric constant material sub-layer, the second low-dielectric constant material sub-layer having at least one different material property than the first low-dielectric constant material sub-layer; and

forming a third low-dielectric constant material sub-layer over the second low-dielectric constant material sub-layer, the third low-dielectric constant material sub-layer having at least one different material property than the second low-dielectric constant material sub-layer.

9. The method according to Claim 8, wherein forming the first ILD layer comprises forming the first low-dielectric constant material sub-layer, second low-dielectric constant material sub-layer, and third low-dielectric constant material sub-layer from methylsilsesquioxane (MSQ), a MSQ derivative, hydridosilsesquioxane (HSQ), a HSQ derivative, an oxide and MSQ hybrid, a porogen/MSQ hybrid, an oxide and HSQ hybrid, a porogen/HSQ hybrid, or combinations thereof.

10. The method according to Claim 8, wherein forming the first ILD layer comprises forming the first low-dielectric constant material sub-layer, second low-dielectric constant material sub-layer, and third low-dielectric constant material sub-layer continuously from the same material in one or more deposition chambers.

11. The method according to Claim 8, wherein forming the first ILD layer comprises forming the first low-dielectric constant material sub-layer, second low-dielectric constant material sub-layer, and third low-dielectric constant material sub-layer while adjusting the deposition conditions.

12. The method according to Claim 8, wherein adjusting the deposition conditions comprises adjusting the gas flow rate, power, or gas species.

13. The method according to Claim 8, wherein the material property of the second low-dielectric constant material sub-layer and the material property of the third low-dielectric constant material sub-layer comprise density, dielectric constant, adhesion, or Young's modulus.

14. The method according to Claim 8, further comprising forming at least one fourth low-dielectric constant material sub-layer over the third low-dielectric constant material sub-layer, the fourth low-dielectric constant material sub-layer having at least one different material property than the third low-dielectric constant material sub-layer.

15. The method according to Claim 8, further comprising;

forming a second etch stop layer over the first ILD layer;

forming a second ILD layer over the second etch stop layer; and

forming at least one second conductive region in the second ILD layer and second etch stop layer, wherein the at least one second conductive region makes electrical contact with at least one first conductive region, and wherein forming the second ILD layer comprises:

forming a fourth low-dielectric constant material sub-layer over the second etch stop layer;

forming a fifth low-dielectric constant material sub-layer over the fourth low-dielectric constant material sub-layer, the fifth low-dielectric constant material sub-layer having at least one different material property than the fourth low-dielectric constant material sub-layer; and

forming a sixth low-dielectric constant material sub-layer over the fifth low-dielectric constant material sub-layer, the sixth low-dielectric constant material sub-layer having at least one different material property than the fifth low-dielectric constant material sub-layer.

16. An inter-level dielectric (ILD) layer of a semiconductor device, comprising:

a first low-dielectric constant material sub-layer, the first low-dielectric constant material having at least one first material property;

a second low-dielectric constant material sub-layer disposed over the first low-dielectric constant material sub-layer, the second low-dielectric constant material sub-layer having at least one second material property, wherein the at least one second material property is different from the at least one first material property; and

a third low-dielectric constant material sub-layer disposed over the second low-dielectric constant material sub-layer, the third low-dielectric constant material sub-layer having at least one third material property, the at least one third material property being different from the at least one second material property.

17. The ILD layer according to Claim 16, wherein the first low-dielectric constant material sub-layer, second low-dielectric constant material sub-layer, and third low-dielectric constant material sub-layer comprise methylsilsesquioxane (MSQ), a MSQ derivative, hydridosilsesquioxane (HSQ), a HSQ derivative, an oxide and MSQ hybrid, a porogen/MSQ hybrid, an oxide and HSQ hybrid, a porogen/HSQ hybrid, or combinations thereof.

18. The ILD layer according to Claim 16, wherein the first low-dielectric constant material sub-layer, second low-dielectric constant material sub-layer, and third low-dielectric constant material sub-layer are formed continuously from the same material in one or more deposition chambers.

19. The ILD layer according to Claim 16, wherein the first material property, second material property, and third material property comprise density, dielectric constant, adhesion, or Young's modulus.

20. The ILD layer according to Claim 16, further comprising at least one fourth low-dielectric constant material sub-layer disposed over the third low-dielectric constant material sub-layer, the fourth low-dielectric constant material sub-layer having at least one fourth material property, wherein the at least one fourth material property is different from the at least one third material property.

21. A semiconductor device, comprising:

a substrate, the substrate having component regions formed thereon;

a first etch stop layer disposed over the substrate;

a first ILD layer disposed over the first etch stop layer; and

at least one first conductive region formed in the first ILD layer and first etch stop layer, wherein at least one first conductive region makes electrical contact with at least one component region of the substrate, and wherein the first ILD layer comprises:

a first low-dielectric constant material sub-layer disposed over the first etch stop layer;

a second low-dielectric constant material sub-layer disposed over the first low-dielectric constant material sub-layer, the second low-dielectric constant material sub-layer having at least one different material property than the first low-dielectric constant material sub-layer; and

a third low-dielectric constant material sub-layer disposed over the second low-dielectric constant material sub-layer, the third low-dielectric constant material sub-layer having at least one different material property than the second low-dielectric constant material sub-layer.

22. The semiconductor device according to Claim 21, wherein the first low-dielectric constant material sub-layer, second low-dielectric constant material sub-layer, and third low-dielectric constant material sub-layer comprise methylsilsesquioxane (MSQ), a MSQ derivative, hydridosilsesquioxane (HSQ), a HSQ derivative, an oxide and MSQ hybrid, a porogen/MSQ hybrid, an oxide and HSQ hybrid, a porogen/HSQ hybrid, or combinations thereof.

23. The semiconductor device according to Claim 21, wherein the first low-dielectric constant material sub-layer, second low-dielectric constant material sub-layer, and third low-dielectric constant material sub-layer are formed continuously from the same material in one or more deposition chambers.

24. The semiconductor device according to Claim 21, wherein the different material property of the second low-dielectric constant material sub-layer and third low-dielectric constant material sub-layer comprises density, dielectric constant, adhesion, or Young's modulus.

25. The semiconductor device according to Claim 21, further comprising at least one fourth low-dielectric constant material sub-layer disposed over the third low-dielectric constant material sub-layer, the fourth low-dielectric constant material sub-layer having at least one different material property than the third low-dielectric constant material sub-layer.

26. The semiconductor device according to Claim 21, further comprising;

a second etch stop layer disposed over the first ILD layer;

a second ILD layer disposed over the second etch stop layer; and

at least one second conductive region disposed in the second ILD layer and second etch stop layer, wherein the at least one second conductive region makes electrical contact with at least one first conductive region, and wherein the first ILD layer comprises:

a fourth low-dielectric constant material sub-layer disposed over the second etch stop layer;

a fifth low-dielectric constant material sub-layer disposed over the fourth low-dielectric constant material sub-layer, the fifth low-dielectric constant material sub-layer having at least one different material property than the fourth low-dielectric constant material sub-layer; and

forming a sixth low-dielectric constant material sub-layer over the fifth low-dielectric constant material sub-layer, the sixth low-dielectric constant material sub-layer having at least one different material property than the fifth low-dielectric constant material sub-layer.

27. The semiconductor device according to Claim 21, wherein the first low-dielectric constant material sub-layer comprises a first Young's modulus, wherein the first Young's modulus is greater than a second Young's modulus of the second low-dielectric constant material sub-layer and a third Young's modulus of the third low-dielectric constant material sub-layer.

28. The semiconductor device according to Claim 21, wherein the first low-dielectric constant material sub-layer comprises a first dielectric constant, wherein the first dielectric constant is greater than a second dielectric constant of the second low-dielectric constant material sub-layer and a third dielectric constant of the third low-dielectric constant material sub-layer.

29. The semiconductor device according to Claim 21, wherein the first low-dielectric constant material sub-layer is more adhesive than the second low-dielectric constant material sub-layer and the third low-dielectric constant material sub-layer.